

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Applicant: Hee Wong
Serial No.: 09/864,561
Filed: May 23, 2001
Due Date: March 4, 2003
Title: METHOD AND APPARATUS FOR ADDRESSING BEAT PATTERNS IN AN INTEGRATED VIDEO DISPLAY SYSTEM

Examiner: R. Laneau
Group Art Unit: 2674
Docket: 50019.54US01/P04766
Confirmation No.: 2859

CERTIFICATE UNDER 37 CFR 1.8:

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, with sufficient postage, in an envelope addressed to: BOX NON-FEE AMENDMENT, Commissioner for Patents, Washington, D.C. 20231 on March 4, 2003.

By: 
Name: John E. Whitaker

BOX NON-FEE AMENDMENT
Commissioner for Patents
Washington, D.C. 20231

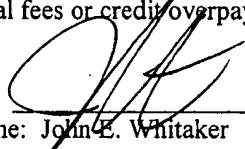
Sir:

We are transmitting herewith the attached:

- ☒ Transmittal Sheet in duplicate containing Certificate of Mailing
- ☒ Amendment, including Version With Markings To Show Changes Made
- ☒ Return postcard

Please consider this a PETITION FOR EXTENSION OF TIME for a sufficient number of months to enter these papers or any future reply, if appropriate. Please charge any additional fees or credit overpayment to Deposit Account No. 13-2725. A duplicate of this sheet is enclosed.

MERCHANT & GOULD P.C.
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206.342.6200

By: 
Name: John E. Whitaker
Reg. No.: 42,222
JW/aj





09/864,561

PATENT

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C/mIN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Hee Wong	Examiner:	R. Laneau
Serial No.:	09/864,561	Group Art Unit:	2674
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited in the United States Postal Service, as first class mail, with sufficient postage, in an envelope addressed to: BOX NON-FEE AMENDMENT, Commissioner for Patents, Washington, D.C. 20231 on March 4, 2003.

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AMENDMENT AND RESPONSE

BOX NON-FEE AMENDMENT
Commissioner for Patents
Washington, D.C. 20231

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Dear Sir:

This Response is submitted in reply to the Office Action dated December 4, 2002. In view of the following amendment and response, Applicant respectfully requests favorable reconsideration of this application.

In the Specification

The paragraph beginning at line 10 of page 6 has been amended as follows:

al
cmt

-- The first operation mode (Scheme A) occurs when the scheme select switch 123 is in the "A" position. In that position, the processed pixel clock signal 117 is coupled to a first D flip-flop 125, a second D flip-flop 127, and to the RGB DAC 129. It will be appreciated that although only a single flip-flop and DAC may be shown in FIGURE 1, there may in fact be